IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

RAMPART ASSET MANAGEMENT LLC,	§	Case No. 6:21-cv-01294
Plaintiff,	§	**JURY TRIAL DEMANDED**
v.	§	
NXP SEMICONDUCTORS N.V., NXP B.V., and NXP SEMICONDUCTORS USA, INC.,	§	
Defendants.	§	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Rampart Asset Management LLC ("Rampart" or "Plaintiff") for its Complaint against Defendants NXP Semiconductors N.V., NXP B.V., and NXP Semiconductors USA, Inc., (collectively, referred to as "NXP" or "Defendants") alleges as follows:

THE PARTIES

1. Rampart is a limited liability company organized and existing under the laws of the State of Texas, with a place of business located at 100 N. 6th Street, Suite 502, Waco, Texas 76701.

2. Upon information and belief, Defendant NXP Semiconductors N.V. ("NXP N.V.") is a corporation organized and existing under the laws of the Netherlands, with its principal place of business located at High Tech Campus 60, Eindhoven 5656 AG, Netherlands.

3. Upon information and belief, Defendant NXP B.V. ("NXP B.V.") is a corporation organized and existing under the laws of the Netherlands, with its principal place of business located at High Tech Campus 60, Eindhoven 5656 AG, Netherlands. NXP N.V. owns one hundred (100) percent of the shares of NXP B.V.

4. Upon information and belief, Defendant NXP Semiconductors USA, Inc. (NXP USA") is registered to do business in Texas and maintains its United States headquarters at 6501 W. William Cannon Drive in Austin, Texas, 78735. NXP B.V. owns one hundred (100) percent of the shares of NXP USA, Inc.

5. Upon information and belief, Defendants NXP USA, Inc. ("NXP USA"), and NXP B.V. ("NXP BV") (collectively, along with NXP N.V., "the NXP Defendants") are subsidiaries of NXP N.V., a global semiconductor company with operations in more than 25 countries, including the United States and, more specifically, Texas.

6. The NXP Defendants are affiliated operating entities. Together with the other subsidiary entities of the parent, NXP N.V., they form a global group (herein, the "NXP Group"), comprising over 50 operating companies.

7. On information and belief, the NXP Defendants are in the business of researching, developing, making, using, and selling semiconductor products, including the NXP-branded products accused of infringement in this case by Rampart (the "Accused Products" defined below).

JURISDICTION

8. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) and 1367.

9. This Court has both general and specific personal jurisdiction over the Defendants consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute. Defendant NXP USA has headquarters in the State of Texas and in this District where it designs, manufactures, markets, and sells its semiconductor products including one or more of the Accused Products. NXP USA has, thereby, committed acts of direct

infringement in the United States and in this District in violation of Rampart's intellectual property rights.

10. Upon information and belief, NXP N.V. and NXP B.V. are companies of the NXP Group that engage in the research, design, manufacture, marketing, sale, offer for sale, and/or provision of technical support, for one or more of the Accused Products. NXP N.V. and NXP B.V. directly sell and facilitate the shipment of the Accused Products to customers in the United States and Texas, including to NXP USA and third-party distributors and end customers. NXP N.V. and NXP B.V. have thereby committed acts of direct infringement in the United States and Texas in violation of Rampart's intellectual property rights.

11. Upon information and belief, NXP B.V. further purposefully and voluntarily placed one or more of the NXP Accused Products into the stream of commerce with the expectation and intent that they will be purchased and used by consumers in Texas, including by (a) selling and/or shipping infringing products to NXP USA and to third-party entities, including into downstream infringing products, with the knowledge and expectation that such products will be imported into the United States and Texas; and (b) directly or indirectly working with other entities within the NXP Group, affiliates, distributors, and other entities located in Texas and abroad, to ensure that infringing products (whether in the form of standalone chips or as integrated into downstream products) reach Texas.

12. Each of the NXP Defendants maintains ongoing and systematic contacts within, and/or has otherwise purposefully directed activities toward, the State of Texas and this District including, but not limited to by: (i) conducting infringing acts in the United States and Texas, (ii) regularly conducting or soliciting business, engaging in other persistent courses of conduct, and/or deriving substantial revenue from goods and services provided to the residents of the United

States and Texas, and/or (iii) by placing infringing products into the stream of commerce with the purpose, intent, and knowledge that they will be used by consumers in the United States and Texas.

13. The NXP Defendants have thus availed themselves of the benefits and privileges of conducting business in the State of Texas and the exercise by this Court of personal jurisdiction over Defendants would not offend traditional notions of fair play and substantial justice.

14. Venue is proper in this District pursuant to 28 U.S.C. §§ 1391(b) and 1400(b). NXP USA maintains regular business operations in this District, and each of the NXP Defendants have committed, and are continuing to commit, acts of infringement in this District and are subject to personal jurisdiction in this District.

15. NXP BV has sufficient minimum contacts with the forum because NXP BV transacts substantial business in the State of Texas and in this Judicial District. Further, NXP BV has, directly or through subsidiaries or intermediaries, committed and continues to commit acts of patent infringement in the State of Texas and in this Judicial District as alleged in this Complaint, as alleged more particularly below.

16. Venue is proper in this Judicial District pursuant to 28 U.S.C. §§ 1391(b) and (c) and 1400(b) because Defendants are subject to personal jurisdiction in this District, have committed acts of patent infringement in this District, and have a regular and established place of business in this District, specifically NXP USA which has its principal place of business located in this District. Defendants, through their own acts and/or through the acts of others, make, , sell, and/or offer to sell infringing products within this District, regularly solicit and do business in this District, and have the requisite minimum contacts with the District such that this venue is a fair and reasonable one. Additionally, venue is proper in any judicial district as to Defendants NXP NV and NXP BV because they are foreign entities. Further, upon information and belief,

Defendants have previously admitted or not contested proper venue in this District in other patent infringement actions.

PATENTS-IN-SUIT

17. On June 14, 2016, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 9,367,248 (the "'248 Patent") entitled "Memory Component with Pattern Register Circuitry to Provide Data Patterns for Calibration." A true and correct copy of the '248 Patent is available at https://pdfpiw.uspto.gov/.piw?PageNum=0&docid=09367248.

18. On August 1, 2017, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 9,721,642 (the "'642 Patent") entitled "Memory Component with Pattern Register Circuitry to Provide Data Patterns for Calibration." A true and correct copy of the '642 Patent is available at https://pdfpiw.uspto.gov/.piw?PageNum=0&docid=09721642.

19. On January 29, 2019, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 10,192,609 (the "'609 Patent") entitled "Memory Component with Pattern Register Circuitry to Provide Data Patterns for Calibration." A true and correct copy of the '609 Patent is available at https://pdfpiw.uspto.gov/.piw?PageNum=0&docid=10192609.

20. On January 6, 2004, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 6,675,272 (the "'272 Patent") entitled "Method and Apparatus for Coordinating Memory Operations Among Diversely-Located Memory Components." A true and correct copy of the '272 Patent is available at https://pdfpiw.uspto.gov/.piw?PageNum=0&docid=06675272.

21. On May 29, 2007, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,225,311 (the "'311 Patent") entitled "Method and Apparatus for Coordinating Memory Operations Among Diversely-Located Memory Components." A true and

correct copy of the '311 Patent is available at https://pdfpiw.uspto.gov/.piw?PageNum=0&docid=07225311.

22. On July 3, 2012, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 8,214,616 (the "'616 Patent") entitled "Memory Controller Device Having Timing Offset Capability." A true and correct copy of the '616 Patent is available at https://pdfpiw.uspto.gov/.piw?PageNum=0&docid=08214616.

23. On June 25, 2013, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 8,472,511 (the "'511 Patent") entitled "Selectable-Tap Equalizer." A true and correct copy of the '511 Patent is available at https://pdfpiw.uspto.gov/.piw?PageNum=0&docid=08472511.

24. Rampart is the sole and exclusive owner of all right, title, and interest in the'248 Patent, the '642 Patent, the '609 Patent, the '272 Patent, the '311 Patent, the '616 Patent, and the '511 Patent, (collectively, the "Patents-in-Suit"), and holds the exclusive right to take all actions necessary to enforce its rights to the Patents-in-Suit, including the filing of this patent infringement lawsuit. Rampart also has the right to recover all damages for past, present, and future infringement of the Patents-in-Suit and to seek injunctive relief as appropriate under the law.

25. Rampart has at all times complied with the marking provisions of 35 U.S.C. § 287 with respect to the Patents-in-Suit.

FACTUAL ALLEGATIONS

26. The Patents-in-Suit generally cover systems and methods for coordinating memory operations and providing data patterns for calibration of memory systems.

27. The '248 Patent generally relates to the field of digital circuits and, more particularly, to an apparatus and method for phase adjustment and memory device signaling

systems. The technology described in the '248 Patent was developed by Craig E. Hampel, Richard E. Perego, Stefanos Sidiropoulos, Ely K. Tsern, and Frederick A. Ware. By way of example, this technology is implemented today in memory systems that adjust the phase of data signals to compensate for phase offset variations between memory devices during normal operation.

28. The '642 Patent generally relates to the field of digital circuits and, more particularly, to an apparatus and method for phase adjustment and memory device signaling systems. The technology described in the '642 Patent was developed by Craig E. Hampel, Richard E. Perego, Stefanos Sidiropoulos, Ely K. Tsern, and Frederick A. Ware. By way of example, this technology is implemented today in memory systems that adjust the phase of data signals to compensate for phase offset variations between memory devices during normal operation.

29. The '609 Patent generally relates to the field of digital circuits and, more particularly, to an apparatus and method for phase adjustment and memory device signaling systems. The technology described in the '609 Patent was developed by Craig E. Hampel, Richard E. Perego, Stefanos Sidiropoulos, Ely K. Tsern, and Frederick A. Ware. By way of example, this technology is implemented today in memory systems that adjust the phase of data signals to compensate for phase offset variations between memory devices during normal operation.

30. The '272 Patent generally relates to information storage and retrieval and, more specifically, to coordinating memory operations among diversely-located memory components. The technology described in the '272 Patent was developed by Frederick A. Ware, Ely K. Tsern, Richard E. Perego, and Craig E. Hampel. By way of example, this technology is implemented today in memory systems that configure multiple memory components to account for address bus and data bus propagation delays.

31. The ’311 Patent generally relates to information storage and retrieval and, more specifically, to coordinating memory operations among diversely-located memory components. The technology described in the ’311 Patent was developed by Frederick A. Ware, Ely K. Tsern, Richard E. Perego, and Craig E. Hampel. By way of example, this technology is implemented today in memory systems that configure multiple memory components to account for address bus and data bus propagation delays.

32. The ’616 Patent generally relates to information storage and retrieval and, more specifically, to coordinating memory operations among diversely-located memory components. The technology described in the ’616 Patent was developed by Frederick A. Ware, Ely K. Tsern, Richard E. Perego, and Craig E. Hampel. By way of example, this technology is implemented today in memory systems that configure multiple memory components to account for address bus and data bus propagation delays.

33. The ’511 Patent generally relates to high speed signaling within and between integrated circuit devices and, more particularly, to reducing latent signal distortions in high speed signaling systems. The technology described in the ’511 Patent was developed by Jared L. Zerbe, Vladimir M. Stojanovic, and Fred F. Chen. By way of example, this technology is implemented today in memory systems that perform iterative testing of signal wires and use pass/fail to correctly set a parameter as part of a write-leveling operation.

34. NXP has infringed and is continuing to infringe one or more of the Patents-in-Suit by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import memory controllers that support one or more of the DDR3, DDR4, DDR5, LPDDR3 and LPDDR4 standards (the “Accused Products”). Such products include, but are not limited to, products in the NXP KLS1023 family, KLS1043 family,

LS1017 family, LS1018 family, LS1020 family, LS1021 family, LS1022 family, LS1023 family, LS1026 family, LS1027 family, LS1028 family, LS1043 family, LS1046 family, LS1048 family, LS1084 family, LS1088 family, LS2044 family, LS2048 family, LS2084 family KS2088 family, LX2080 family, LX2082 family, LX2120 family, LX2122 family, LX2160 family, LX2162 family, MIMX8MD family, MIMX8ML family, MIMX8MM family, MIMX8MN family, MIMX8MQ family, and the PIMX8MQ family.

COUNT I
(Infringement of the '248 Patent)

35. Paragraphs 1 through 34 are incorporated by reference as if fully set forth herein.

36. Rampart has not licensed or otherwise authorized Defendants to make, use, offer for sale, sell, or import any products that embody the inventions of the '248 Patent.

37. Defendants have and continue to directly infringe the '248 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting DDR4 external memories, such as the NXP KLS1023 family, KLS1043 family, LS1017 family, LS1018 family, LS1020 family, LS1021 family, LS1022 family, LS1023 family, LS1026 family, LS1027 family, LS1028 family, LS1043 family, LS1046 family, LS1048 family, LS1084 family, LS1088 family, LS2044 family, LS2048 family, LS2084 family KS2088 family, LX2080 family, LX2082 family, LX2120 family, LX2122 family, LX2160 family, LX2162 family, MIMX8MD family, MIMX8ML family, MIMX8MM family, MIMX8MN family, MIMX8MQ family, and the PIMX8MQ family.

38. For example, Defendants have and continue to directly infringe at least claim 1 of the '248 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR4 standard. For example,

members of the NXP LS1046A family include DDR4 external memory controllers capable of controlling a memory system consisting of DDR4 SDRAMs, each of which is compliant with the JEDEC standard JESD79-4D, as shown by the QorIQ LS1046A, LS1026A Data Sheet (Document Number LS1046A, Rev. 4, 06/2020):

QorIQ LS1046A, LS1026A Data Sheet

Features

- LS1046A has four cores and LS1026A has two cores
- Four 32-bit/64-bit Arm® Cortex®-v8 A72 CPUs
  - Arranged as a single cluster of four cores sharing a single 2 MB L2 cache
  - Up to 1.8 GHz operation
  - Single-threaded cores with 32 KB L1 data cache and 48 KB L1 instruction cache
- Hierarchical interconnect fabric
  - Up to 700 MHz operation
- One 32-bit/64-bit DDR4 SDRAM memory controller with ECC and interleaving support
  - Up to 2.1 GT/s

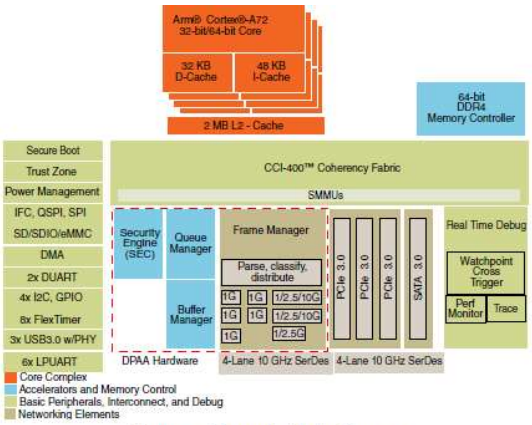


Figure 1. LS1046A block diagram

3.9.2 DDR4 SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 memories. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

39. The required characteristics of DDR4 memories and memory systems and therefore of DDR4 memory controllers and their encompassing integrated circuits are defined by JEDEC in a collection of publicly available standards. In particular, standard JESD79-4 is the standard defining DDR4 SDRAMs, and JESD79-4D is the latest version of that standard, dated July 2021:

This document defines the DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 2 Gb through 16 Gb for x4, x8, and x16 DDR4 SDRAM devices. This standard was created based on the DDR3 standards (JESD79-3) and some aspects of the DDR and DDR2 standards (JESD79, JESD79-2).

JESD79-4D page 1.

40. The Accused Products including DDR4 memory controllers include a first circuit to transmit commands to the memory component, the commands including a read command that specifies data to be accessed from a memory core of the memory component. DDR4 SDRAM

memory controllers, including members of the NXP LS1046A family, include a first circuit which is a driver circuit that sends commands to the DDR4 SDRAMs over signal traces (e.g., D1_MACT_B, D1_MRAS_B, D1_MCAS_B, D1_MWE_B):

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MACT_B	Activate	D28	O	$G1V_{DD}$	---
D1_MCAS_B	Column Address Strobe / MA[15]	AC28	O	$G1V_{DD}$	---
D1_MRAS_B	Row Address Strobe / MA[16]	AA28	O	$G1V_{DD}$	---
D1_MWE_B	Write Enable / MA[14]	AB28	O	$G1V_{DD}$	---

JESD79-4 refers to these signals at the SDRAMs as ACT_n, RAS_n/A16, CAS_n/A15, and WE_n/A14.

2.7 Pinout Description

Table 3 — Pinout Description

Symbol	Type	Function
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table

JESD79-4D p. 5.

A read command is specified by setting ACT_n High.

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write commands.
[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

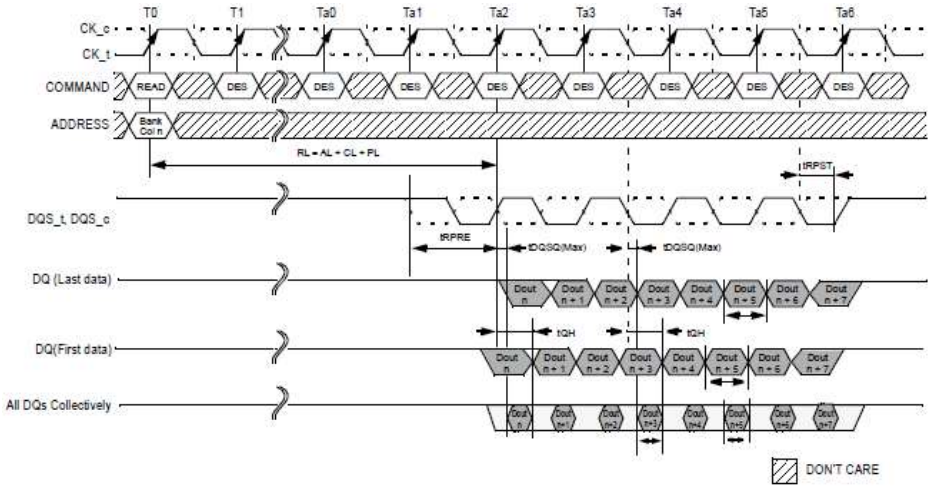
Table 35 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

JESD79-4D, p. 29

41. The Accused Products including DDR4 memory controllers include circuits that drive these command signals toward the DDR4 SDRAMs. Among the commands that DDR4 SDRAMs can respond to are read commands. A read command is provided to a DDR4 SDRAM by sending a command in which ACT_n is H, RAS_n/A16 is H, CAS_n/A15 is L, and WE_n/A14 is H, where H and L represent voltage levels representing logic states, as defined in Section 8 of JESD79-4. A read command presented to a DDR4 SDRAM causes it to convey addressed memory

location to its pins for conveyance to the memory controller, as described in Section 4.24 of JESD79-4:



42. Additionally, the Accused Products including DDR4 memory controllers include a second circuit to receive data sent by the memory component via an external bus, the data sent by the memory component in response to the read command. A read command presented to a collection of DDR4 SDRAMs by DDR4 SDRAM memory controllers, including members of the NXP LS1046A family, causes the DDR4 SDRAM to convey an addressed memory location to its pins for conveyance to the memory controller, as described in Section 4.24 of JESD79-4. The Accused Products, including the LS1046A, necessarily have a second circuit to receive the data being sent from the memory component as a result of a read command.

43. Additionally, the Accused Products including DDR4 memory controllers include calibration circuitry, operable during calibration, to receive at least a first data pattern and a second data pattern from the memory component. DDR4 SDRAMs, including members of the NXP LS1046A family, include a calibration mode called DQ Read Training. Read Training is performed as part of power-up initialization:

3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization and is shown in Figure 7.

1. Apply power (RESET_n and TEN are recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained below 0.2 x VDD for minimum 200us with stable power and TEN needs to be maintained below 0.2 x VDD for minimum 700us with stable power. CKE is pulled "Low" anytime before RESET_n being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and $(V_{DD}-V_{DDQ}) < 0.3$volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.

15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).

JESD79-4D, pp 11-12.

44. Read DQ Training is the mechanism by which the members of the NXP LS1046A family adjust their receive timing to reliably capture read data from the memory components. The circuitry that calibrates the DQ receivers is the claimed calibration circuitry.

45. Additionally, the Accused Products including DDR4 memory controllers include pattern register circuitry. The Multi-Purpose Register (MPR) is a collection of 4 8-bit registers that provide the data source for DQ Training data patterns. The contents of at least two of the MPRs are the first data pattern and the second data pattern in the memory component. During DQ Training, values of the MPR registers are communicated from the DDR4 SDRAM memory components to the memory controller on the DQ external bus in response to one of the commands.

4.10.3 MPR Reads

MPR reads are supported using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR reads.

In MPR Mode:

Reads (back-to-back) from Page 0 may use tCCD_S or tCCD_L timing between read commands; Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between read commands; tCCD_L must be used for timing between read commands

MPR reads using BC4:

BA1 and BA0 indicate the MPR location within the selected page in MPR Mode.

A10 and other address pins are don't care including BG1 and BG0.

Read commands for BC4 are supported with starting column address of A2:A0 of '000' and '100'.

Data Bus Inversion (DBI) is not allowed during MPR Read operation. During MPR Read, DRAM ignores Read DBI Enable setting in MR5 bit A12 in MPR mode.

DDR4 MPR mode is enabled by programming bit A2=1 and then reads are done from a specific MPR location.
MPR location is specified with the Read command using Bank address bits BA1 and BA0.

Each MPR location is 8 bit wide.

JESD79-4D, p. 44.

46. Defendants have and continue to indirectly infringe one or more claims of the '248 Patent by knowingly and intentionally inducing others, including NXP customers and end-users,

to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

47. Upon information and belief, with knowledge and intent, or with willful blindness, Defendants encourage and facilitate infringement of one or more claims of the ’248 Patent by others, including at least claim 1. For example, Rambus Inc. notified NXP in August 2018 that NXP was infringing the’248 Patent by making, using, selling, offering to sell, and/or importing products, including the LS1046A family, that include controllers for DDR3, DDR4, LPDDR3, or LPDDR4 memories.

48. Defendants, with knowledge that these products, or the use thereof, infringe the ’248 Patent at least as of August 2018, knowingly and intentionally induced, and continue to knowingly and intentionally induce, direct infringement of the ’248 Patent by providing these products to end-users for use in an infringing manner.

49. Rampart has suffered damages as a result of Defendants’ direct and indirect infringement of the ’248 Patent in an amount to be proved at trial.

50. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendants’ infringement of the ’248 Patent for which there is no adequate remedy at law, unless Defendants’ infringement is enjoined by this Court.

51. NXP has committed and continues to commit acts of infringement that NXP actually knew or should have known constituted an unjustifiably high risk of infringement of at least one valid and enforceable claim of the ’248 Patent. NXP’s direct and indirect infringement of the ’248 Patent has been and continues to be willful, intentional, deliberate, and/or in conscious disregard of Rampart’s rights under the patent. Rampart is entitled to an award of treble damages, reasonable attorney fees, and costs in bringing this action.

COUNT II
(Infringement of the ’642 Patent)

52. Paragraphs 1 through 34 are incorporated by reference as if fully set forth herein.

53. Rampart has not licensed or otherwise authorized Defendants to make, use, offer for sale, sell, or import any products that embody the inventions of the ’642 Patent.

54. Defendants have and continue to directly infringe the ’642 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting DDR4 external memories, such as the NXP KLS1023 family, KLS1043 family, LS1017 family, LS1018 family, LS1020 family, LS1021 family, LS1022 family, LS1023 family, LS1026 family, LS1027 family, LS1028 family, LS1043 family, LS1046 family, LS1048 family, LS1084 family, LS1088 family, LS2044 family, LS2048 family, LS2084 family KS2088 family, LX2080 family, LX2082 family, LX2120 family, LX2122 family, LX2160 family, LX2162 family, MIMX8MD family, MIMX8ML family, MIMX8MM family, MIMX8MN family, MIMX8MQ family, and the PIMX8MQ family.

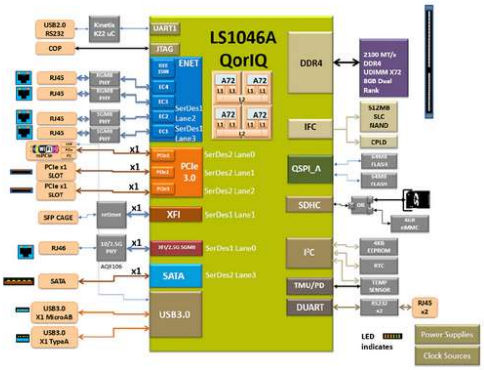
55. For example, Defendants have and continue to directly infringe at least claim 1 of the ’642 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR4 standard. For example, members of the NXP LS1046A family include DDR4 external memory controllers capable of controlling a memory system consisting of DDR4 SDRAMs, each of which is compliant with the JEDEC standard JESD79-4D, as shown by the QorIQ LS1046A, LA1026A Data Sheet (Document Number LS1046A, Rev. 4, 06/2020):

QorIQ LS1046A, LS1026A Data Sheet

Features

- LS1046A has four cores and LS1026A has two cores
- Four 32-bit/64-bit Arm® Cortex®-v8 A72 CPUs
  - Arranged as a single cluster of four cores sharing a single 2 MB L2 cache
  - Up to 1.8 GHz operation
  - Single-threaded cores with 32 KB L1 data cache and 48 KB L1 instruction cache
- Hierarchical interconnect fabric
  - Up to 700 MHz operation
- One 32-bit/64-bit DDR4 SDRAM memory controller with ECC and interleaving support
  - Up to 2.1 GT/s

Layerscape LS1046A Reference Design Board



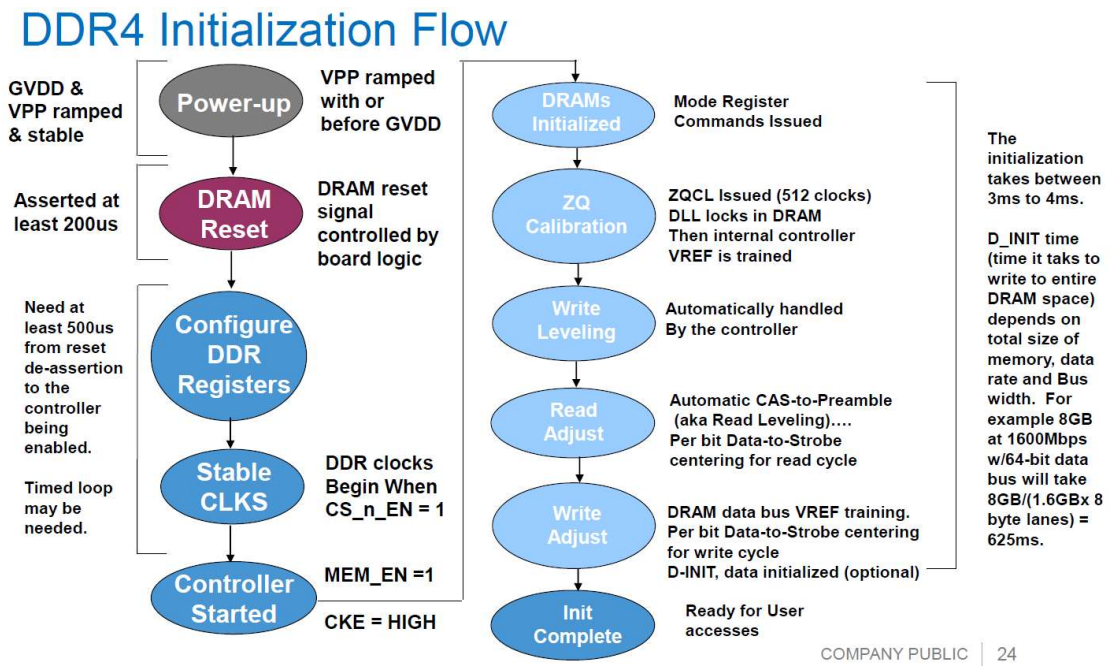
3.9.2 DDR4 SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 memories. Note that the required $GV_{DD}(typ)$ voltage is 1.2 V when interfacing to DDR4 SDRAM.

56. The required characteristics of DDR4 memories and memory systems and therefore of DDR4 memory controllers and their encompassing integrated circuits are defined by JEDEC in a collection of publicly available standards. In particular, standard JESD79-4 is the standard defining DDR4 SDRAMs, and JESD79-4D is the latest version of that standard, dated July 2021. Controller DQ Training (sometimes called Read Leveling) is performed as a necessary step in the initialization of a DDR4 memory system. The provisions provided in the SDRAMs for the purposes of facilitating DQ Training are documented in the JEDEC standards.

This document defines the DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 2 Gb through 16 Gb for x4, x8, and x16 DDR4 SDRAM devices. This standard was created based on the DDR3 standards (JESD79-3) and some aspects of the DDR and DDR2 standards (JESD79, JESD79-2).

JESD79-4D page 1.



Overcoming DDR Challenges in High-Performance Design, September 2018, AMF-NET-T3267, https://community.nxp.com/pwmxy87654/attachments/pwmxy87654/tech-days/289/1/AMF-NET-T3267.pdf

57. The Accused Products including DDR4 memory controllers include a first circuit to transmit commands to the memory component, the commands including a read command that specifies data to be accessed from a memory core of the memory component. DDR4 SDRAM memory controllers, including members of the NXP LS1046A family, include a first circuit which is a driver circuit that sends commands to the DDR4 SDRAMs over signal traces (e.g., D1_MACT_B, D1_MRAS_B, D1_MCAS_B, D1_MWE_B):

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MACT_B	Activate	D28	O	$G1V_{DD}$	---

D1_MCAS_B	Column Address Strobe / MA[15]	AC28	O	$G1V_{DD}$	---
D1_MRAS_B	Row Address Strobe / MA[16]	AA28	O	$G1V_{DD}$	---
D1_MWE_B	Write Enable / MA[14]	AB28	O	$G1V_{DD}$	---

JESD79-4 refers to these signals at the SDRAMs, as ACT_n, RAS_n/A16, CAS_n/A15, and WE_n/A14.

2.7 Pinout Description

Table 3 — Pinout Description

Symbol	Type	Function
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table

JESD79-4D page 5.

A read command is specified by setting ACT_n High.

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write commands.
[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

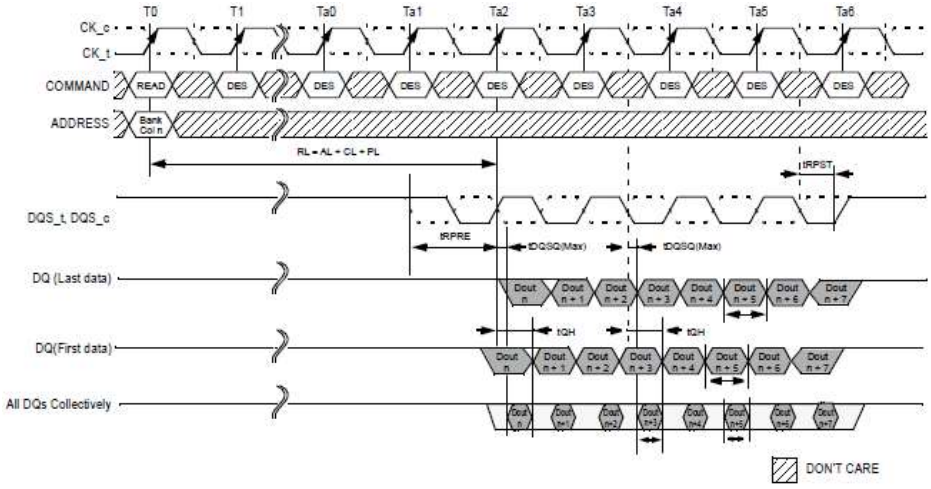
Table 35 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

JESD79-4D, p. 29

58. The Accused Products including DDR4 memory controllers include circuits that drive these command signals toward the DDR4 SDRAMs. Among the commands that DDR4 SDRAMs can respond to are read commands. A read command is provided to a DDR4 SDRAM by sending a command in which ACT_n is H, RAS_n/A16 is H, CAS_n/A15 is L, and WE_n/A14 is H, where H and L represent voltage levels representing logic states, as defined in section 8 of JESD79-4. A read command presented to a DDR4 SDRAM causes it to convey an addressed

memory location to its pins for conveyance to the memory controller, as described in Section 4.24 of JESD79-4:



59. Additionally, the Accused Products including DDR4 memory controllers include a second circuit to receive data sent by the memory component via an external bus, the data sent by the memory component in response to the read command. A read command presented to a DDR4 SDRAM by DDR4 SDRAM memory controllers, including members of the NXP LS1046A family, causes the DDR4 SDRAM to convey an addressed memory location to its pins for conveyance to the memory controller, as described in Section 4.24 of JESD79-4. The Accused Products, including the LS1046A, necessarily have a second circuit to receive the data being sent from the memory component as a result of a read command.

60. Additionally, the Accused Products including DDR4 memory controllers include calibration circuitry, operable during calibration, to receive from the memory component, in response to one of the commands, a pattern selected from at least one of a first data pattern and a second data pattern and to, based on the selected pattern, adjust a timing of a timing reference signal for sampling the data at the second receive circuit, wherein the timing of the timing reference signal is initially set using an initial calibration sequence and then updated during one or more

subsequent calibration sequences. DDR4 SDRAMs, including members of the NXP LS1046A family, include a calibration mode called DQ Training (also known as Read Leveling). Read Training is performed as part of power-up initialization:

3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization and is shown in Figure 7.

1. Apply power (RESET_n and TEN are recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained below 0.2 x VDD for minimum 200us with stable power and TEN needs to be maintained below 0.2 x VDD for minimum 700us with stable power. CKE is pulled "Low" anytime before RESET_n being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and $(V_{DD}-V_{DDQ}) < 0.3$volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.

15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).

JESD79-4D, pp. 11-12.

61. Read DQ Training is the mechanism by which the members of the NXP LS1046A family adjust their receive timing to reliably capture read data from the memory components. The circuitry that calibrates the DQ receivers is the claimed calibration circuitry.

62. Additionally, the Accused Products including DDR4 memory controllers include pattern register circuitry. The Multi-Purpose Register (MPR) is a collection of 4 8-bit registers that provide the data source for DQ Training data patterns. The contents of at least two of the MPRs are the first data pattern and the second data pattern in the memory component. During DQ Training, values of the MPR registers are communicated from the DDR4 SDRAM memory components to the memory controller on the DQ external bus in response to one of the commands.

4.10.3 MPR Reads

MPR reads are supported using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR reads.

In MPR Mode:

Reads (back-to-back) from Page 0 may use tCCD_S or tCCD_L timing between read commands; Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between read commands; tCCD_L must be used for timing between read commands

MPR reads using BC4:

BA1 and BA0 indicate the MPR location within the selected page in MPR Mode.

A10 and other address pins are don't care including BG1 and BG0.

Read commands for BC4 are supported with starting column address of A2:A0 of '000' and '100'.

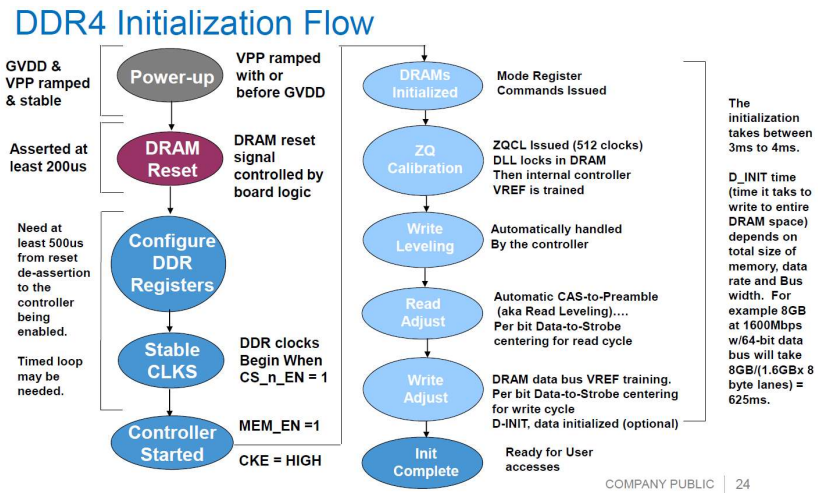
Data Bus Inversion (DBI) is not allowed during MPR Read operation. During MPR Read, DRAM ignores Read DBI Enable setting in MR5 bit A12 in MPR mode.

DDR4 MPR mode is enabled by programming bit A2=1 and then reads are done from a specific MPR location.
MPR location is specified with the Read command using Bank address bits BA1 and BA0.

Each MPR location is 8 bit wide.

JESD79-4D, p. 44.

63. Additionally, the Accused Products including DDR4 memory controllers, including members of the LS1046A family, include DQ Training to adjust a timing of a timing reference signal for sampling the data at the second receive circuit. The MPR data sequences are used during the DQ Training (Read Leveling) phase of initialization. DQ Training facilitates proper capture of read data from the DDR4 SDRAM by the memory controller at very high frequencies of operation.



Overcoming DDR Challenges in High-Performance Design, September 2018, AMF-NET-T3267, https://community.nxp.com/pwmxy87654/attachments/pwmxy87654/tech-days/289/1/AMF-NET-T3267.pdf

64. Additionally, the Accused Products including DDR4 memory controllers, including members of the LS1046A family, include a timing reference signal, wherein the timing of the timing reference signal is initially set using an initial calibration sequence and then updated during one or more subsequent calibration sequences. It is known that initialization and calibration of the DDR4 SDRAM memory controller to DDR4 SDRAM interface is necessary and required. It is also necessary to recalibrate the interface periodically and/or on detection of an error or on

recognition shift in the conditions (principally temperature and voltage) under which the memory system is operating.

65. Defendants have and continue to indirectly infringe one or more claims of the ’642 Patent by knowingly and intentionally inducing others, including NXP customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

66. Upon information and belief, with knowledge and intent, or with willful blindness, Defendants encourage and facilitate infringement of one or more claims of the ’642 Patent by others, including at least claim 1. For example, Rambus Inc. notified NXP in August 2018 that NXP was infringing the ’248 Patent by making, using, selling, offering to sell, and/or importing products, including the LS1046A family, that include controllers for DDR3, DDR4, LPDDR3 or LPDDR4 memories. The ’642 Patent is a continuation of the ’248 Patent and is part of the same Patent family. Based on the 2018 disclosure of the ’248 Patent, NXP was notified or willfully blind to the fact that the ’642 Patent infringes NXP products.

67. Defendants, with knowledge that these products, or the use thereof, infringe the ’642 Patent at least as of August 2018, knowingly and intentionally induced, and continue to knowingly and intentionally induce, direct infringement of the ’642 Patent by providing these products to end-users for use in an infringing manner.

68. Rampart has suffered damages as a result of Defendants’ direct and indirect infringement of the ’642 Patent in an amount to be proved at trial.

69. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendants’ infringement of the ’642 Patent, for which there is no adequate remedy at law, unless Defendants’ infringement is enjoined by this Court.

70. NXP has committed and continues to commit acts of infringement that NXP actually knew or should have known constituted an unjustifiably high risk of infringement of at least one valid and enforceable claim of the ’642 Patent. NXP’s direct and indirect infringement of the ’642 Patent has been and continues to be willful, intentional, deliberate, and/or in conscious disregard of Rampart’s rights under the patent. Rampart is entitled to an award of treble damages, reasonable attorney fees, and costs in bringing this action.

COUNT III
(Infringement of the ’609 Patent)

71. Paragraphs 1 through 34 are incorporated by reference as if fully set forth herein.

72. Rampart has not licensed or otherwise authorized Defendants to make, use, offer for sale, sell, or import any products that embody the inventions of the ’609 Patent.

73. Defendants have and continue to directly infringe the ’609 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting DDR4 external memories, such as the NXP KLS1023 family, KLS1043 family, LS1017 family, LS1018 family, LS1020 family, LS1021 family, LS1022 family, LS1023 family, LS1026 family, LS1027 family, LS1028 family, LS1043 family, LS1046 family, LS1048 family, LS1084 family, LS1088 family, LS2044 family, LS2048 family, LS2084 family KS2088 family, LX2080 family, LX2082 family, LX2120 family, LX2122 family, LX2160 family, LX2162 family, MIMX8MD family, MIMX8ML family, MIMX8MM family, MIMX8MN family, MIMX8MQ family, and the PIMX8MQ family.

74. For example, Defendants have and continue to directly infringe at least claim 1 of the ’609 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR4 standard. For example,

members of the NXP LS1046A family include DDR4 external memory controllers capable of controlling a memory system consisting of DDR4 SDRAMs, each of which is compliant with the JEDEC standard JESD79-4D, as shown by the QorIQ LS1046A, LS1026A Data Sheet (Document Number LS1046A, Rev. 4, 06/2020):

QorIQ LS1046A, LS1026A Data Sheet

Features

- LS1046A has four cores and LS1026A has two cores
- Four 32-bit/64-bit Arm® Cortex®-v8 A72 CPUs
  - Arranged as a single cluster of four cores sharing a single 2 MB L2 cache
  - Up to 1.8 GHz operation
  - Single-threaded cores with 32 KB L1 data cache and 48 KB L1 instruction cache
- Hierarchical interconnect fabric
  - Up to 700 MHz operation
- One 32-bit/64-bit DDR4 SDRAM memory controller with ECC and interleaving support
  - Up to 2.1 GT/s

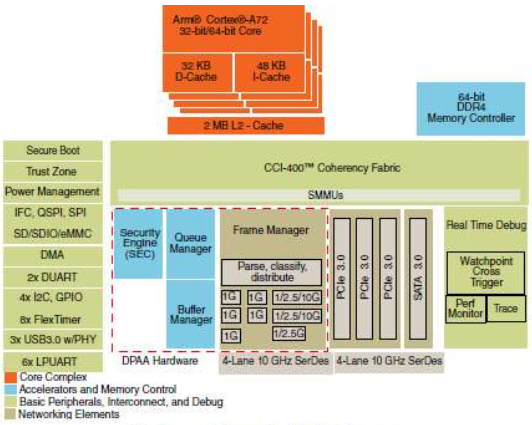


Figure 1. LS1046A block diagram

3.9.2 DDR4 SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 memories. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

75. The required characteristics of DDR4 memories and memory systems and therefore of DDR4 memory controllers and their encompassing integrated circuits are defined by JEDEC in a collection of publicly available standards. In particular, standard JESD79-4 is the standard defining DDR4 SDRAMs, and JESD79-4D is the latest version of that standard, dated July 2021:

This document defines the DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 2 Gb through 16 Gb for x4, x8, and x16 DDR4 SDRAM devices. This standard was created based on the DDR3 standards (JESD79-3) and some aspects of the DDR and DDR2 standards (JESD79, JESD79-2).

JESD79-4D page 1.

76. The Accused Products including DDR4 memory controllers include a first circuit to transmit commands to the memory component. DDR4 SDRAM memory controllers, including members of the NXP LS1046A family, include a first circuit which is a driver circuit that sends

commands to the DDR4 SDRAMs over signal traces (e.g., D1_MACT_B, D1_MRAS_B, D1_MCAS_B, D1_MWE_B):

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MACT_B	Activate	D28	O	$G1V_{DD}$	---
D1_MCAS_B	Column Address Strobe / MA[15]	AC28	O	$G1V_{DD}$	---
D1_MRAS_B	Row Address Strobe / MA[16]	AA28	O	$G1V_{DD}$	---
D1_MWE_B	Write Enable / MA[14]	AB28	O	$G1V_{DD}$	---

JESD79-4 refers to these signals at the SDRAMs, as ACT_n, RAS_n/A16, CAS_n/A15, and WE_n/A14.

2.7 Pinout Description

Table 3 — Pinout Description

Symbol	Type	Function
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table

JESD79-4D page 5.

A read command is specified by setting ACT_n High.

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write commands.
[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

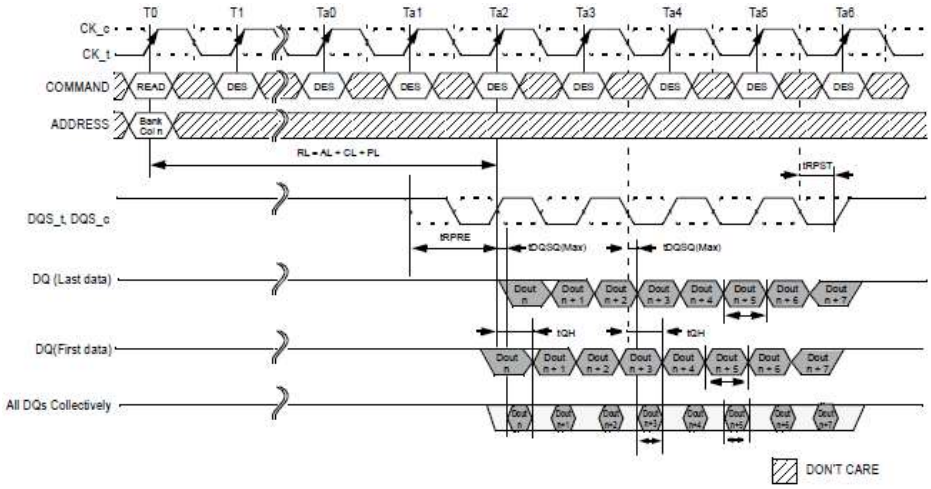
Table 35 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

JESD79-4D, p. 29

77. The Accused Products including DDR4 memory controllers include circuits that drive these command signals toward the DDR4 SDRAMs. Among the commands that DDR4 SDRAMs can respond to are read commands. A read command is provided to a DDR4 SDRAM by sending a command in which ACT_n is H, RAS_n/A16 is H, CAS_n/A15 is L, and WE_n/A14 is H, where H and L represent voltage levels representing logic states, as defined in Section 8 of JESD79-4. A read command presented to a DDR4 SDRAM causes it to convey an addressed

memory locations to its pins for conveyance to the memory controller, as described in Section 4.24 of JESD79-4:

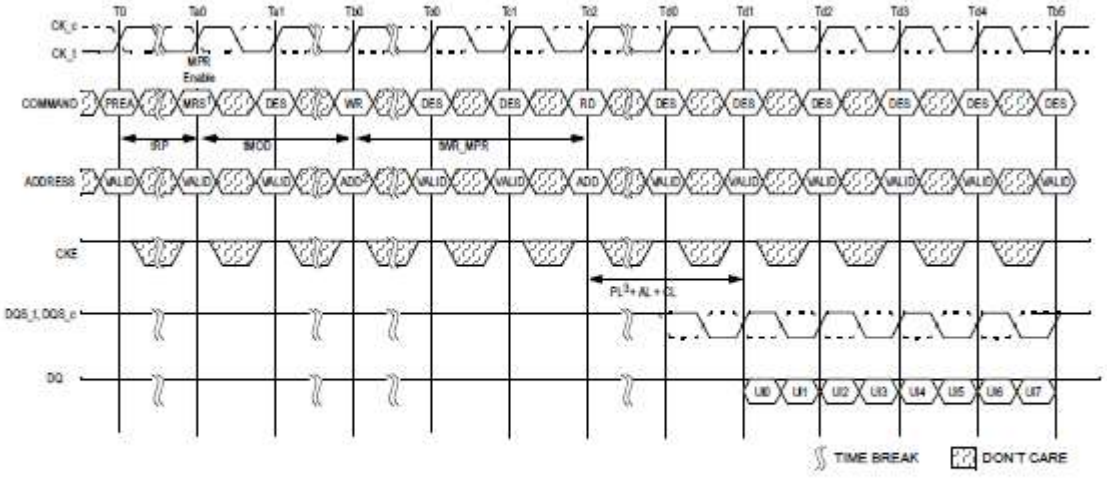


78. Additionally, the Accused Products including DDR4 memory controllers initiate a first command that specifies a first data pattern to be stored in a first register of the memory component. DDR4 SDRAMs, including DDR4 SDRAMs used with members of the NXP LS1046A family, include a Multi-Purpose Register (MPR) for storing bit patterns for use in initialization/channel calibration. Each of the four (4) MPR registers can be written by write command (WR) after the SDRAM is placed into appropriate mode, as indicated by a write into Mode Register 3 (MR3). During such a write command, as indicated at time Tb0, address signals BA1 and BA0 indicate which MPR register is to be written with the specified bit pattern provided on A[7:0]. The Accused Products, including the LS1046A, perform a write command writing a first one of the four MPR registers, which is a first command that specifies a first data pattern to be stored in a first register of the memory component.

79. Additionally, the Accused Products including DDR4 memory controllers initiate a second command that specifies a second data pattern to be stored in a second register of the memory component. DDR4 SDRAMs, connected to members of the NXP LS1046A family,

include a second MPR register storing a second bit pattern (subsequent to the writing of a first MPR register with a first bit pattern). The second MPR register is addressed by the BA1 and BA0 address bits in conjunction with the Write command:

4.10.4 MPR Writes (cont'd)

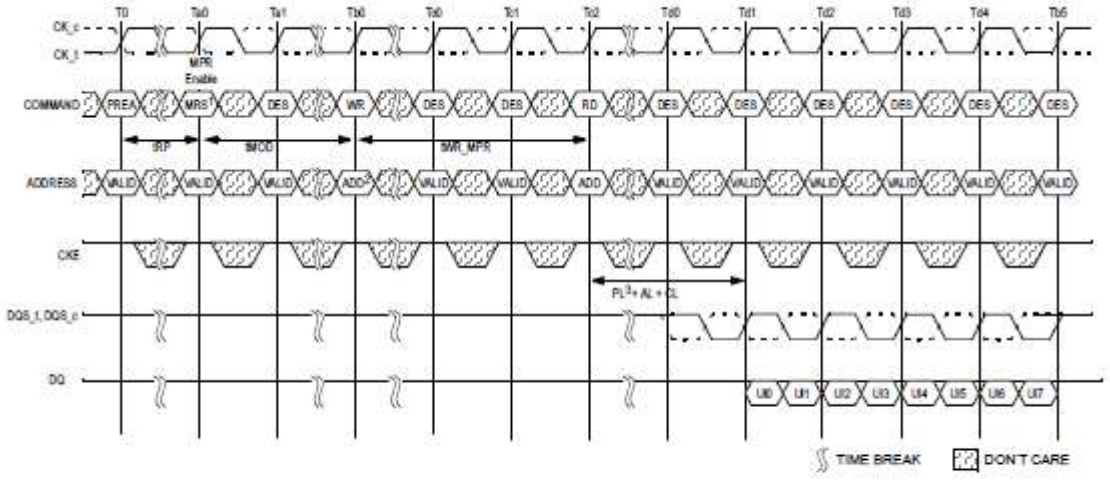


NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
NOTE 2 Address setting - BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.
NOTE 3 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

JESD79-4D, p. 47.

80. Additionally, the Accused Products including DDR4 memory controllers initiate a third command to select one of the first data pattern or the second data pattern to be output by the memory component. The contents of the MPR registers are read out with read commands (RD) onto the DQ lines for use in DQ Training. Once the MR3 A2 bit is set to 0, a selected one of the first data pattern and the second data pattern is transmitted by the memory component from an MPR register onto the external bus in response to a RD (read) command. One such command is illustrated below as being provided to the memory component at time Tb0.

4.10.4 MPR Writes (cont'd)



NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
NOTE 2 Address setting - BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.
NOTE 3 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

4.10.3 MPR Reads

MPR reads are supported using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR reads.

In MPR Mode:

Reads (back-to-back) from Page 0 may use tCCD_S or tCCD_L timing between read commands; Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between read commands; tCCD_L must be used for timing between read commands

MPR reads using BC4:

BA1 and BA0 indicate the MPR location within the selected page in MPR Mode.

A10 and other address pins are don't care including BG1 and BG0.

Read commands for BC4 are supported with starting column address of A2:A0 of '000' and '100'.

Data Bus Inversion (DBI) is not allowed during MPR Read operation. During MPR Read, DRAM ignores Read DBI Enable setting in MR5 bit A12 in MPR mode.

DDR4 MPR mode is enabled by programming bit A2=1 and then reads are done from a specific MPR location.
MPR location is specified with the Read command using Bank address bits BA1 and BA0.

Each MPR location is 8 bit wide.

JESD79-4D, p. 44.

81. Defendants have and continue to indirectly infringe one or more claims of the '609 Patent by knowingly and intentionally inducing others, including NXP customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

82. Upon information and belief, with knowledge and intent, or with willful blindness, Defendants encourage and facilitate infringement of one or more claims of the '609 Patent by others, including at least claim 1. For example, Rambus Inc. notified NXP in August 2018 that

NXP was infringing the ’248 Patent by making, using, selling, offering to sell, and/or importing products, including the LS1046A family, that include controllers for DDR3, DDR4, LPDDR3, or LPDDR4 memories. The ’609 Patent is a continuation of the ’248 Patent and is part of the same Patent family. Based on the 2018 disclosure of the ’248 Patent, NXP was notified or willfully blind to the fact that the ’609 Patent infringes NXP products.

83. Defendants, with knowledge, or at least willfully blind that these products, or the use thereof, infringe the ’609 Patent at least as of January 2019, knowingly and intentionally induced, and continue to knowingly and intentionally induce, direct infringement of the ’609 Patent by providing these products to end-users for use in an infringing manner.

84. Rampart has suffered damages as a result of Defendants’ direct and indirect infringement of the ’609 Patent in an amount to be proved at trial.

85. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendants’ infringement of the ’609 Patent for which there is no adequate remedy at law, unless Defendants’ infringement is enjoined by this Court.

86. NXP has committed and continues to commit acts of infringement that NXP actually knew or should have known constituted an unjustifiably high risk of infringement of at least one valid and enforceable claim of the ’609 Patent. NXP’s direct and indirect infringement of the ’609 Patent has been and continues to be willful, intentional, deliberate, and/or in conscious disregard of Rampart’s rights under the patent. Rampart is entitled to an award of treble damages, reasonable attorney fees, and costs in bringing this action.

COUNT IV
(Infringement of the ’272 Patent)

87. Paragraphs 1 through 34 are incorporated by reference as if fully set forth herein.

88. Rampart has not licensed or otherwise authorized Defendants to make, use, offer for sale, sell, or import any products that embody the inventions of the ’272 Patent.

89. Defendants have and continue to directly infringe the ’272 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting the DDR4 external memories, such as the NXP KLS1023 family, KLS1043 family, LS1017 family, LS1018 family, LS1020 family, LS1021 family, LS1022 family, LS1023 family, LS1026 family, LS1027 family, LS1028 family, LS1043 family, LS1046 family, LS1048 family, LS1084 family, LS1088 family, LS2044 family, LS2048 family, LS2084 family KS2088 family, LX2080 family, LX2082 family, LX2120 family, LX2122 family, LX2160 family, LX2162 family, MIMX8MD family, MIMX8ML family, MIMX8MM family, MIMX8MN family, MIMX8MQ family, and the PIMX8MQ family.

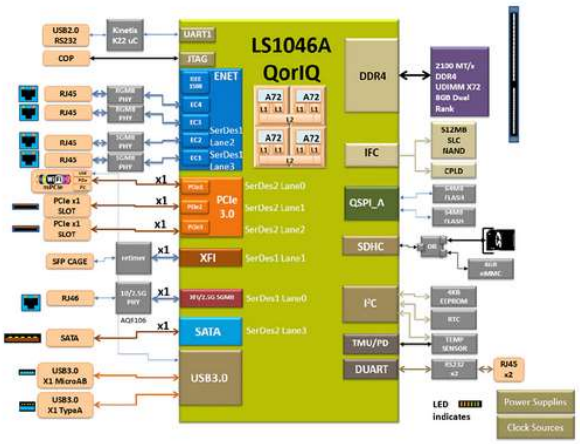
90. For example, Defendants have and continue to directly infringe at least claim 26 of the ’272 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR4 standard. For example, members of the NXP LS1046A family include DDR4 external memory controllers capable of conducting memory operations in a memory system consisting of DDR4 SDRAMs, each of which is compliant with the JEDEC standard JESD79-4D, as shown by the QorIQ LS1046A, LS1026A Data Sheet (Document Number LS1046A, Rev. 4, 06/2020):

Layerscape LS1046A Reference Design Board

QorIQ LS1046A, LS1026A Data Sheet

Features

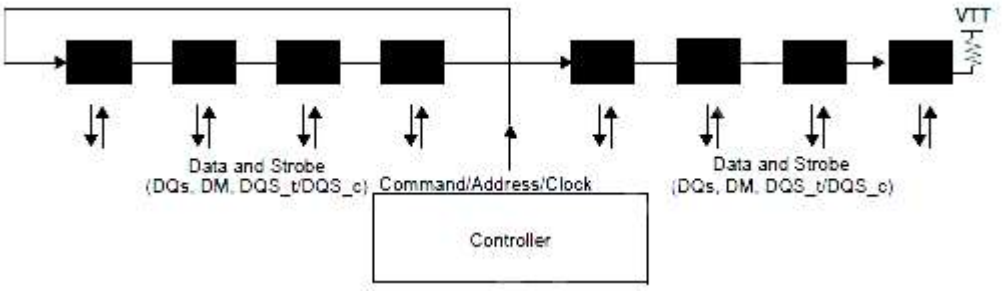
- LS1046A has four cores and LS1026A has two cores
- Four 32-bit/64-bit Arm® Cortex®-v8 A72 CPUs
  - Arranged as a single cluster of four cores sharing a single 2 MB L2 cache
  - Up to 1.8 GHz operation
  - Single-threaded cores with 32 KB L1 data cache and 48 KB L1 instruction cache
- Hierarchical interconnect fabric
  - Up to 700 MHz operation
- One 32-bit/64-bit DDR4 SDRAM memory controller with ECC and interleaving support
  - Up to 2.1 GT/s



3.9 DDR4 SDRAM controller

This section describes the DC and AC electrical specifications for the DDR4 SDRAM controller interface. Note that the required G1V_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

91. The Accused Products perform a method of conducting memory operations in a memory system comprising a memory controller component and a rank of memory components comprising slices, the slices comprising a first slice and a second slice. DDR4 SDRAM memory controllers, including members of the NXP LS1046A family, are necessarily connected to a collection of DDR4 SDRAMs that constitute a 32- or 64-bit wide memory subsystem connected via an identically sized memory bus. Each 8-bit subsection of the memory subsystem connected to the LS1046A, and bus, constitute a slice. One of said slices is a first slice and another is a second slice.



JEDEC DDR4 SDRAM UDIMM Design Specification, Revision 1.22 p. 4. 20.26-18

92. The Accused Products including DDR4 memory controllers perform a method of conducting memory operations in a memory system comprising a memory controller component wherein the memory controller component is coupled to conductors, the conductors including a common address bus coupling the memory controller component to the first slice and the second slice. The memory bus connecting the DDR4 memory controller in the LS1046A family to the DDR4 SDRAMs consists in part of 32 or 64 conductors for conveying data between the two, as well as conductors for conveying address and control signals. The memory controller is coupled to these conductors. Among the signals exiting DDR4 memory controllers including those in the LS1046A family, for the controlling the DDR4 SDRAMs are a collection of address signals which convey address signals to all the DDR4 SDRAMs in the memory subsystem, including the DDR4 SDRAMs that constitute the first and second slices.

2.2 Pinout list

This table provides the pinout listing for the LS1046A by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	V27	O	$G1V_{DD}$	---
D1_MA01	Address	N27	O	$G1V_{DD}$	---
D1_MA02	Address	N28	O	$G1V_{DD}$	---
D1_MA03	Address	M28	O	$G1V_{DD}$	---
D1_MA04	Address	L28	O	$G1V_{DD}$	---
D1_MA05	Address	L27	O	$G1V_{DD}$	---
D1_MA06	Address	K28	O	$G1V_{DD}$	---
D1_MA07	Address	J27	O	$G1V_{DD}$	---
D1_MA08	Address	J28	O	$G1V_{DD}$	---
D1_MA09	Address	G28	O	$G1V_{DD}$	---
D1_MA10	Address	Y28	O	$G1V_{DD}$	---
D1_MA11	Address	H28	O	$G1V_{DD}$	---
D1_MA12	Address	G27	O	$G1V_{DD}$	---
D1_MA13	Address	AD27	O	$G1V_{DD}$	---

QorIQ LS1046A, LS1026A Data sheet, p. 10-13.

93. Additionally, the Accused Products including DDR4 memory controllers perform a method for conducting memory operations in a memory system comprising a memory controller component wherein a first data bus couples the memory controller component to the first slice,

and a second data bus couples the memory controller component to the second slice, the first data bus being separate from the second data bus. Among the signals connecting the DDR4 memory controller in the LS1046A to the SDRAMs are data signals coupling bits 0 through 7 of the DDR SDRAM data bus (D1_MDQ[00:07]) leaving the LS1046A to the DDR4 SDRAMs in the first slice of memory components. Among the signals connecting the DDR4 memory controller in the LS1046A to the SDRAMs are data signals coupling bits 24 through 31 of the DDR SDRAM data bus (D1_MDQ[24-31]) leaving the LS1046A to the DDR4 SDRAMs in the second slice of memory components. The first and second data buses connecting the DDR4 memory controller in the LS1046A to the memory components in the first and second slices are entirely separate.

94. Additionally, the Accused Products including DDR4 memory controllers include the method comprising the step of providing said memory system, providing a signal to one of the conductors, the signal selected from a group consisting of an address signal, a write data signal, and a read data signal. The LS1046A requires a main memory consisting of DDR4 SDRAMs connected to the DDR4 SDRAM memory controller resident on the LS1046A to be provided externally to the LS1046A. In order to operate the DDR4 SDRAMs in the rank of DDR4 SDRAMs attached to the LS1046A, the DDR4 memory controller must provide address, control, and write data to the DDR4 SDRAMs via the memory bus. In particular, the A15 address signal is placed on the conductor called CAS_n/A15 on the DDR4 SDRAM side, A15/CAS_n in the DDR4 SDRAM UDIMM specification, and D1_MCAS_B in the pin definition of the LS1046A.

2.2 Pinout list

This table provides the pinout listing for the LS1046A by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					

D1_MCAS_B	Column Address Strobe / MA[15]	AC28	O	$G1V_{DD}$	---

QorIQ LS1046A, LS1026A Data sheet, p. 10.

Table 4 — Input/Output Functional Description

Symbol	Type	I/O Level	Function
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	VDD	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table.

JEDEC DDR4 SDRAM UDIMM Design Specification, Revision 1.22 p. 4.20.26-8

2.7 Pinout Description

Table 3 — Pinout Description

Symbol	Type	Function
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table

JESD79-4D, p. 5.

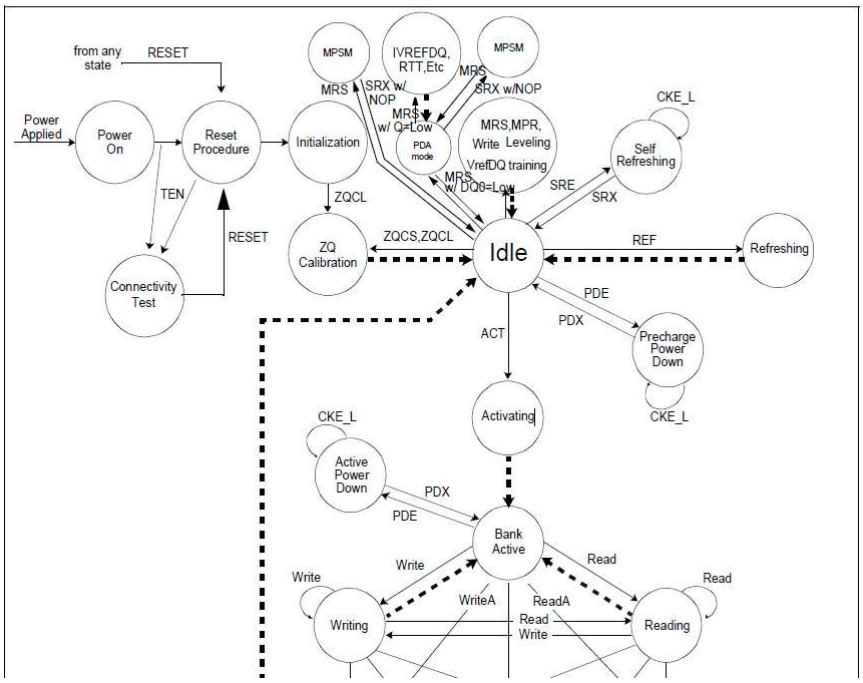
95. Additionally, the Accused Products including DDR4 memory controllers initiate the method wherein the propagation delay of one of the conductors is longer than an amount of time that an element of information represented by the signal is applied to the conductor. The DDR4 Memory Controller in the LS1046A is capable of operation at up to 2.1 GT/s on the data bus and half that on the address bus. At 2.1 GT/s, the clock period, and therefore the address bit residency on an address conductor is 952ps. The propagation velocity of signals on digital systems built on printed circuit boards is generally less than 6 in/ns. Therefore, if the address signal conductor is longer than approximately 5.7 inches, then the address conductor carrying the A15 address signal has a propagation delay that is longer than the amount of time that the address signal bit is present on the conductor at this frequency. When the memory system is constructed of DIMMs, including UDIMMs, or if the DDR4 SDRAMs are placed on the same printed circuit

board as the LS1046A, but placed and interconnected in a comparable manner as in the UDIMMs, then the minimum conductor length used by the A15 address signal is substantially greater than 5.7 inches. In these DDR4 SDRAM DIMMs, the clock, command, and address signal conductors are routed from its connector location along the edge of the module to one of the left or right edges of the module, and then across the full width of the module. The DDR4 SDRAM UDIMM modules are 133.35 mm (about 5.25 inches). Accounting for this width, additional trace length on the module and the path from the LS1046A to the module, the minimum length of the conductor carrying the A15 address signal is necessarily greater than 5.7 inches.

96. Additionally, the Accused Products including DDR4 memory controllers include the method for conducting memory operations in a memory system comprising the step of using the signal to conduct the memory operations. The address signal A15 is required to fully specify Activate commands which are a necessary prerequisite to read and write operations in an DDR4 SDRAM-based memory system.

3.1 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than on bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.



JESD79-4D, p. 10

97. Defendants have and continue to indirectly infringe one or more claims of the ’272 Patent by knowingly and intentionally inducing others, including NXP customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

98. Upon information and belief, with knowledge and intent, or with willful blindness, Defendants encourage and facilitate infringement of one or more claims of the ’272 Patent by others, including at least claim 26. For example, Rambus Inc. notified Freescale in June 2013 that Freescale was infringing the’272 Patent by making, using, selling, offering to sell, and/or importing products, including the LS1_FamilyA15, that include controllers for DDR3 and DDR4 memories. NXP therefore had knowledge or was willfully blind to the infringing use of the ’272 Patent.

99. Defendants, with knowledge that these products, or the use thereof, infringe the '272 Patent at least as of June 2013, knowingly and intentionally induced, and continue to knowingly and intentionally induce, direct infringement of the '272 Patent by providing these products to end-users for use in an infringing manner.

100. Defendants induced infringement by others, including end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end-users, infringe the '272 Patent, but while remaining willfully blind to the infringement.

101. Rampart has suffered damages as a result of Defendants' direct and indirect infringement of the '272 Patent in an amount to be proved at trial.

102. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendants' infringement of the '272 Patent for which there is no adequate remedy at law, unless Defendants' infringement is enjoined by this Court.

103. NXP has committed and continues to commit acts of infringement that NXP actually knew or should have known constituted an unjustifiably high risk of infringement of at least one valid and enforceable claim of the '272 Patent. NXP's direct and indirect infringement of the '272 Patent has been and continues to be willful, intentional, deliberate, and/or in conscious disregard of Rampart's rights under the patent. Rampart is entitled to an award of treble damages, reasonable attorney fees, and costs in bringing this action.

COUNT V
(Infringement of the '311 Patent)

104. Paragraphs 1 through 34 are incorporated by reference as if fully set forth herein.

105. Rampart has not licensed or otherwise authorized Defendants to make, use, offer for sale, sell, or import any products that embody the inventions of the '311 Patent.

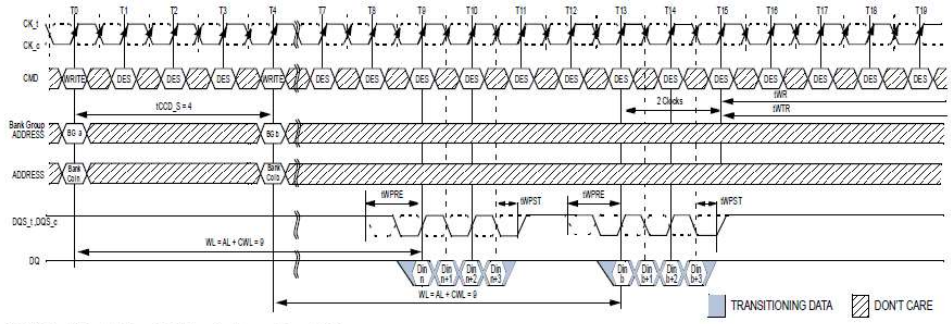
106. Defendants have and continue to directly infringe the '311 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting the DDR4 external memories, such as the NXP KLS1023 family, KLS1043 family, LS1017 family, LS1018 family, LS1020 family, LS1021 family, LS1022 family, LS1023 family, LS1026 family, LS1027 family, LS1028 family, LS1043 family, LS1046 family, LS1048 family, LS1084 family, LS1088 family, LS2044 family, LS2048 family, LS2084 family KS2088 family, LX2080 family, LX2082 family, LX2120 family, LX2122 family, LX2160 family, LX2162 family, MIMX8MD family, MIMX8ML family, MIMX8MM family, MIMX8MN family, MIMX8MQ family, and the PIMX8MQ family.

107. For example, Defendants have and continue to directly infringe at least claim 26 of the '311 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR4 standard. For example, members of the NXP LS1046A family include DDR4 external memory controllers capable of controlling a memory system consisting of DDR4 SDRAM controllers, each of which is compliant with the JEDEC standard JESD79-4D.

108. The Accused Products including DDR4 memory controllers include a first transmitter to output first control information synchronously with respect to a first transition of a timing signal and second control information synchronously with respect to a second transition of the timing signal. DDR4 SDRAM memory controllers, connected to members of the LS1046A family, include a collection of control signals which provide control information to the memory devices to direct their operation. A set of control information is sent synchronously with the memory clock signal, which is the timing signal. Subsequently, a second set of control information

is sent along the same control information signal lines synchronously with respect to a second transition of the memory clock.

109. Additionally, the Accused Products including DDR4 memory controllers send first control information indicating a first write operation to a first memory device, such that the first memory device samples first data in response to the first control information. If the first control information specifies a write operation, the first memory device will, at the appropriate time, sample first data arriving on a set of data signal lines from the memory controller.



NOTE 1 BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK
NOTE 2 DIN n (or b) = data-in to column n(or column b).
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T15.

Figure 136 — WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Different Bank Group

JESD79-4D, p. 126.

110. Additionally, the Accused Products including DDR4 memory controllers send second control information indicating a second write operation to a second memory device, such that the second memory device samples second data in response to the second control information. DDR4 SDRAM memory controllers connected to members of the LS1046A family, send a second write to the same rank of memory devices causing a second memory device to sample the second data in response to the second control information.

111. Additionally, the Accused Products including DDR4 memory controllers include a second transmitter to output the first data using a first timing offset that is based on a first time that

the first control information takes to propagate from the first transmitter to the first memory device. DDR4 SDRAM memory controllers including members of the LS1046A family include a second transmitter that is connected to a first data signal conductor connecting the LS1046A memory controller to the first memory device for transmitting a first data to the first memory device. In DDR4 SDRAM memory controllers connected to members of the LS1046A family, the control information follows the same path as the memory clock, and so the timing offset for sending the first data is based on both the propagation delay of the memory clock and the control information.

112. Additionally, the Accused Products including DDR4 memory controllers include a third transmitter to output the second data using a second timing offset that is based on a second time that the second control information takes to propagate from the first transmitter to the second memory device, the second time being longer than the first time. DDR4 SDRAM memory controllers including members of the LS1046A family include a third transmitter that is connected to a second data signal conductor connecting the LS1046A memory controller to the second memory device for transmitting a second data to the second memory device. A DDR4 SDRAM memory system, such as one built using a DDR4 SDRAM UDIMM, comprises control information following the same path as the memory clock, so that the timing offset for sending the second data is based on both the propagation delay of the memory clock and the control information. The DDR4 SDRAM memory system comprises the propagation delay of clock and control information travelling together which are different to different memory devices. Therefore, the second memory device is one of the pair such that the second time is longer than the first time.

113. Defendants have and continue to indirectly infringe one or more claims of the ’311 Patent by knowingly and intentionally inducing others, including NXP customers and end-users,

to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

114. Upon information and belief, with knowledge and intent, or with willful blindness, Defendants encourage and facilitate infringement of one or more claims of the ’311 Patent by others, including at least claim 26 For example, Rambus Inc. notified NXP in August 2018 that NXP was infringing the’311 Patent by making, using, selling, offering to sell, and/or importing products, including the LS1046A family, that include controllers for DDR3, DDR4, LPDDR3 or LPDDR4 memories.

115. Defendants, with knowledge that these products, or the use thereof, infringe the ’311 Patent at least as of August 2018, knowingly and intentionally induced, and continue to knowingly and intentionally induce, direct infringement of the ’311 Patent by providing these products to end-users for use in an infringing manner.

116. Defendants induced infringement by others, including end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end-users, infringe the ’311 Patent, but while remaining willfully blind to the infringement.

117. Rampart has suffered damages as a result of Defendants’ direct and indirect infringement of the ’311 Patent in an amount to be proved at trial.

118. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendants’ infringement of the ’311 Patent, for which there is no adequate remedy at law, unless Defendants’ infringement is enjoined by this Court.

119. NXP has committed and continues to commit acts of infringement that NXP actually knew or should have known constituted an unjustifiably high risk of infringement of at

least one valid and enforceable claim of the '311 Patent. NXP's direct and indirect infringement of the '311 Patent has been and continues to be willful, intentional, deliberate, and/or in conscious disregard of Rampart's rights under the patent. Rampart is entitled to an award of treble damages, reasonable attorney fees, and costs in bringing this action.

COUNT VI
(Infringement of the '616 Patent)

120. Paragraphs 1 through 34 are incorporated by reference as if fully set forth herein.

121. Rampart has not licensed or otherwise authorized Defendants to make, use, offer for sale, sell, or import any products that embody the inventions of the '616 Patent.

122. Defendants have and continue to directly infringe the '616 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting the DDR4 external memories, such as the NXP KLS1023 family, KLS1043 family, LS1017 family, LS1018 family, LS1020 family, LS1021 family, LS1022 family, LS1023 family, LS1026 family, LS1027 family, LS1028 family, LS1043 family, LS1046 family, LS1048 family, LS1084 family, LS1088 family, LS2044 family, LS2048 family, LS2084 family KS2088 family, LX2080 family, LX2082 family, LX2120 family, LX2122 family, LX2160 family, LX2162 family, MIMX8MD family, MIMX8ML family, MIMX8MM family, MIMX8MN family, MIMX8MQ family, and the PIMX8MQ family.

123. For example, Defendants have and continue to directly infringe at least claim 36 of the '616 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR4 standard. For example, members of the NXP LS1046A family include DDR4 external memory controllers capable of

controlling a memory system consisting of DDR4 SDRAMs, each of which is compliant with the JEDEC standard JESD79-4D.

124. The Accused Products including DDR4 memory controllers include a clock buffer to provide a clock signal to an external clock line routed in succession to a first and second memory component. DDR4 SDRAM memory controllers, connected to members of the LS1046A family, include a buffer that drives the memory clock signal onto the D1_MCK0 pins and the external clock line toward the plurality of DDR4 SDRAMs that necessarily include a first and second memory components. The same would be the case if the DDR4 SDRAMs are mounted directly on the same printed circuit board as the LS1046A if a comparable clock distribution strategy was used within the memory subsystem.

125. Additionally, the Accused Products including DDR4 memory controllers include a memory controller component wherein a first propagation time required for the clock signal to propagate on the clock line from the memory controller component to the first memory component is shorter than a second propagation time required for the clock signal to propagate on the clock line from the memory controller component to the second memory component. In DDR4 SDRAM UDIMMs, the clock signal traverses the DIMM from one SDRAM near one edge to the last SDRAM near the opposite edge. Those edges are specified to be 133mm apart. Based on this or any comparable clock distribution topology, the first propagation time required for the clock to propagate from the memory controller to the first memory component will be shorter than the second clock propagation time from the memory controller to the second memory component.

126. Additionally, the Accused Products including DDR4 memory controllers include a first transmitter to transmit first data along a first dedicated data bus to the first memory component. DDR4 SDRAM memory controllers connected to members of the NXP LS1046A

family are connected to the plurality of data signal conductors connecting the LS1046A memory controller to the first memory component for transmitting a first data to the first memory component.

127. Additionally, the Accused Products including DDR4 memory controllers include a second transmitter to transmit second data along a second dedicated data bus to the second memory component. DDR4 SDRAM memory controllers, connected to members of the NXP LS1046A family are connected to the plurality of data signal conductors connecting the LS1046A memory controller to the second memory component for transmitting a second data to the second memory component.

128. Additionally, the Accused Products including DDR4 memory controllers comprise a memory controller component wherein the time at which the second data is transmitted is offset from a time at which the first data is transmitted based, at least in part, on the difference between the first and second propagation times. In DDR4 SDRAM memory controllers including members of the NXP LS1046A family, write leveling is applied to adjust the time write data is transmitted towards each respective memory component so that the data arrives approximately coincidently with the clock signal traveling along the clock line. Thus, after write leveling has been performed as part of memory system initialization, the time the second data is sent toward the second memory component is offset from the time the first data by an amount approximately equal to the difference in the clock propagation times.

14. Wait for both tDLLK and tZQ init to be completed
15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).
16. Optional MBIST PPR mode can be entered by setting MR4:A0 to a "1", followed by subsequent MR0 guard key sequences, then

JESD79-4D, p. 12.

4.7 Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR4 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. This feature may not be required under some system conditions provided the host can maintain the tDQSS, tDSS and tDSH specifications.

The memory controller can use the 'write leveling' feature and feedback from the DDR4 SDRAM to adjust the DQS_t - DQS_c to CK_t - CK_c relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS_t - DQS_c to align the rising edge of DQS_t - DQS_c with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK_t - CK_c, sampled with the rising edge of DQS_t - DQS_c, through the DQ bus. The controller repeatedly delays DQS_t - DQS_c until a transition from 0 to 1 is detected. The DQS_t - DQS_c delay established through this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS_t - DQS_c signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 15.

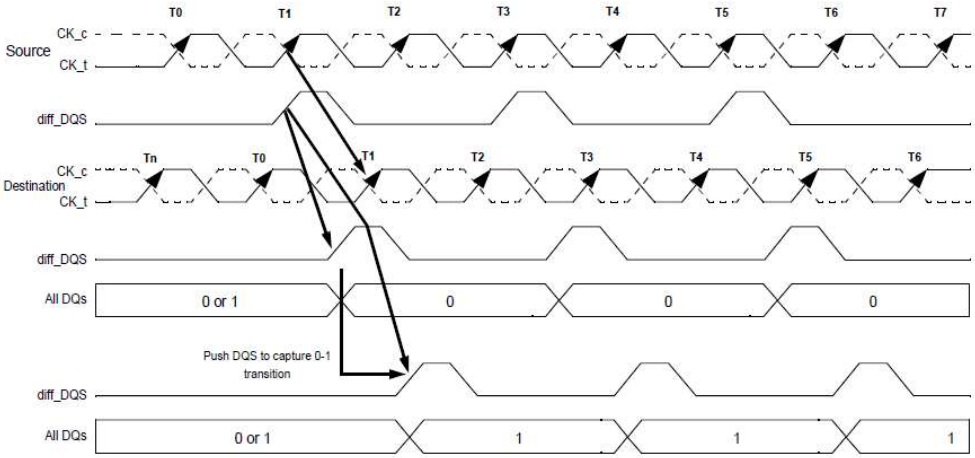


Figure 15 — Write Leveling Concept

JESD79-4D, p. 36.

129. Additionally, the Accused Products including DDR4 memory controllers include a third transmitter to transmit a first strobe signal along a first dedicated strobe signal line to the first memory component, wherein the first memory component receives the first strobe signal to sample the first data. DDR4 SDRAM memory controllers, including members of the NXP LS1046A family, include data lines, wherein each 8 data lines has associated with them a single differential data strobe signal. The DDR4 external memory controller part of the LS1046A includes a transmitter for sending a first dedicated data strobe signal on a first dedicated strobe signal line

that is associated with the data signals/lines going to the first memory component. The first DDR4 SDRAM memory component uses the received strobe signal to sample the first data.

130. Additionally, the Accused Products including DDR4 memory controllers include a fourth transmitter to transmit a second strobe signal along a second dedicated strobe signal line to the second memory component, wherein the second memory component receives the second strobe signal to sample the second data. DDR4 SDRAM memory controllers including those connected to members of the NXP LS1046A family include a second DDR4 SDRAM memory component using the received strobe signal to sample the second data. DDR4 SDRAM memory controllers, including members of the NXP LS1046A family, include data lines, wherein each 8 data lines has associated with them a single differential data strobe signal. The DDR4 external memory controller part of the LS1046A includes a transmitter for sending a second data strobe signal on a second dedicated strobe signal line that is associated with the data signals/lines going to the second memory component. The second DDR4 SDRAM memory component uses the received strobe signal to sample the second data.

131. Additionally, the Accused Products including DDR4 memory controllers transmit the second strobe signal at a time that is offset from a time at which the first strobe signal is transmitted based, at least in part, on the difference between the first and second propagation times. In DDR4 SDRAM memory controllers connected to members of the NXP LS1046A family, the time the second strobe signal is sent is offset from the time the first strobe is sent, comparably to the offset between when the first data is sent and when the second data is sent.

132. Defendants have and continue to indirectly infringe one or more claims of the ’616 Patent by knowingly and intentionally inducing others, including NXP customers and end-users,

to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling and/or importing into the United States the Accused Products.

133. Upon information and belief, with knowledge and intent, or with willful blindness, Defendants encourage and facilitate infringement of one or more claims of the ’616 Patent by others, including at least claim 36. For example, Rambus Inc. notified NXP in August 2018 that NXP was infringing the’616 Patent by making, using, selling, offering to sell and/or importing products, including the LS1046A family, that include controllers for DDR3, DDR4, LPDDR3 or LPDDR4 memories.

134. Defendants, with knowledge that these products, or the use thereof, infringe the ’616 Patent at least as of August 2018, knowingly and intentionally induced, and continue to knowingly and intentionally induce, direct infringement of the ’616 Patent by providing these products to end users for use in an infringing manner.

135. Defendants induced infringement by others, including end users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end users, infringe the ’616 Patent, but while remaining willfully blind to the infringement.

136. Rampart has suffered damages as a result of Defendants’ direct and indirect infringement of the ’616 Patent in an amount to be proved at trial.

137. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendants’ infringement of the ’616 Patent, for which there is no adequate remedy at law, unless Defendants’ infringement is enjoined by this Court.

138. NXP has committed and continues to commit acts of infringement that NXP actually knew or should have known constituted an unjustifiably high risk of infringement of at

least one valid and enforceable claim of the '616 Patent. NXP's direct and indirect infringement of the '616 Patent has been and continues to be willful, intentional, deliberate, and/or in conscious disregard of Rampart's rights under the patent. Rampart is entitled to an award of treble damages, reasonable attorney fees, and costs in bringing this action.

COUNT VII
(Infringement of the '511 Patent)

139. Paragraphs 1 through 34 are incorporated by reference as if fully set forth herein.

140. Rampart has not licensed or otherwise authorized Defendants to make, use, offer for sale, sell, or import any products that embody the inventions of the '511 Patent.

141. Defendants have and continue to directly infringe the '511 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting DDR4 external memories, such as the NXP KLS1023 family, KLS1043 family, LS1017 family, LS1018 family, LS1020 family, LS1021 family, LS1022 family, LS1023 family, LS1026 family, LS1027 family, LS1028 family, LS1043 family, LS1046 family, LS1048 family, LS1084 family, LS1088 family, LS2044 family, LS2048 family, LS2084 family KS2088 family, LX2080 family, LX2082 family, LX2120 family, LX2122 family, LX2160 family, LX2162 family, MIMX8MD family, MIMX8ML family, MIMX8MM family, MIMX8MN family, MIMX8MQ family, and the PIMX8MQ family.

142. For example, Defendants have and continue to directly infringe at least claim 1 of the '511 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR4 standard. For example, members of the NXP LS1046A family include DDR4 external memory controllers capable

of conducting memory operations in a memory system consisting of DDR4 SDRAMs, each of which is compliant with the JEDEC standard JESD79-4D.

143. The Accused Products including DDR4 memory controllers perform a method of setting a parameter in an integrated circuit receiver to a value selected from a set of possible values, the integrated circuit receiver to receive a signal from a conductive signal path. Products containing DDR4 memory controllers, including members of the LS1046A family, are connected to the DDR4 SDRAMs under their control in part via the DQ lines that are part of the memory bus. The DDR4 memory controller therein includes connections to a 64-bit memory bus. The DDR4 SDRAMs respond to commands from the DDR4 memory controller in the LS1046A. Part of the initialization of the memory system by the memory controller in DDR4 memory controllers, including the LS1046A family, is a procedure called VrefDQ Training. In VrefDQ Training, memory controller iteratively causes the DDR4 SDRAMs to adjust, via writes to the SDRAM's mode registers, the SDRAM's internally generated VrefDQ voltage which is used in the DQ receivers in the SDRAMs during the capturing of data values arriving on the DQ signal lines from the memory controller. A DDR4 SDRAM in the memory system is an integrated circuit. The VrefDQ voltage is set in the SDRAM to a value set by the memory controller writing specific bit patterns into Mode Register 6 (MR6) bits 7:0 (VrefDQ Training Range and VrefDQ Training Value).

2.2 Pinout list

This table provides the pinout listing for the LS1046A by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MDQ00	Data	C22	IO	$G1V_{DD}$	---
D1_MDQ01	Data	A23	IO	$G1V_{DD}$	---
D1_MDQ02	Data	C26	IO	$G1V_{DD}$	---
D1_MDQ03	Data	A27	IO	$G1V_{DD}$	---
D1_MDQ04	Data	B22	IO	$G1V_{DD}$	---
D1_MDQ05	Data	A22	IO	$G1V_{DD}$	---
D1_MDQ06	Data	B25	IO	$G1V_{DD}$	---
D1_MDQ07	Data	A26	IO	$G1V_{DD}$	---
D1_MDQ54	Data	AD22	IO	$G1V_{DD}$	---
D1_MDQ55	Data	AE22	IO	$G1V_{DD}$	---
D1_MDQ56	Data	AH25	IO	$G1V_{DD}$	---
D1_MDQ57	Data	AF24	IO	$G1V_{DD}$	---
D1_MDQ58	Data	AG22	IO	$G1V_{DD}$	---
D1_MDQ59	Data	AF22	IO	$G1V_{DD}$	---
D1_MDQ60	Data	AH26	IO	$G1V_{DD}$	---
D1_MDQ61	Data	AG25	IO	$G1V_{DD}$	---
D1_MDQ62	Data	AF23	IO	$G1V_{DD}$	---
D1_MDQ63	Data	AH22	IO	$G1V_{DD}$	---

QorIQ LS1046A, LS1026A Data sheet, p. 10-12.

Each of these DQ pins is coupled to a receiver within the DDR4 SDRAM.

Table 3 — Pinout Description (Cont'd)

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JESD79-4D, p. 6.

3.5 Mode Register (cont'd)

MR6

Table 31 — Mode Register 6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13, A9, A8	RFU	
A12:A10	tCCD_L	(see Table 32)
A7	VrefDQ Training Enable	0 = Disable (Normal operation Mode) 1 = Enable (Training Mode)
A6	VrefDQ Training Range	(see Table 33)
A5:A0	VrefDQ Training Value	(see Table 34)

JESD79-4D, p. 27.

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Voent_DQ(midpoint), in order to have valid Rx Mask values.

Voent_DQ(midpoint) is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 229. This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.

JESD79-4D, p. 250.

4.13 DQ Vref Training (cont'd)

The Vref increment/decrement step times are defined by Vref_time. The Vref_time is defined from t0 to t1 as shown in the Figure 30 below where t1 is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance (Vref_val_tol).

The Vref valid level is defined by Vref_val tolerance to qualify the step time t1 as shown in Figure 32 through Figure 35. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

Vref_time is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change in Vref voltage

t0 - is referenced to MRS command clock
t1 - is referenced to the Vref_val_tol

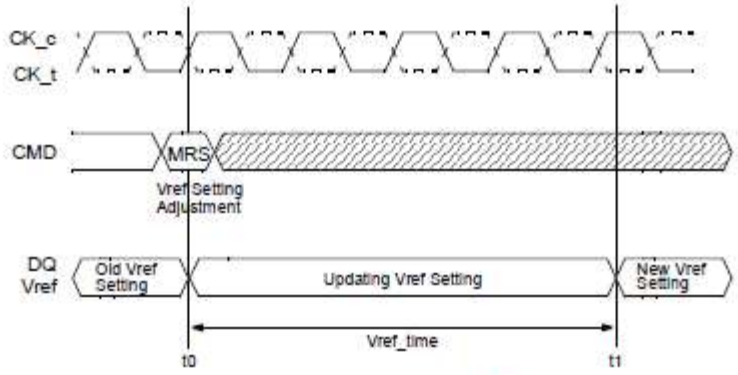
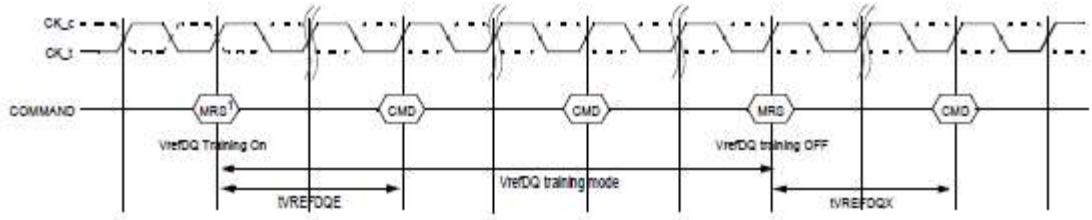


Figure 30 — Vref_time timing diagram

JESD79-4D, p. 59.

144. The Accused Products including DDR4 memory controllers cause the DDR4 SDRAMs to sample the conductive signal path with a sampling circuit of the integrated circuit receiver while iteratively setting the parameter to be different values in the set, to produce digital samples. As part of the Vref DQ Training procedure, each of the DDR4 SDRAMs that are part of the memory system receive write commands and sample the DQ conductive signal paths with the input receivers coupled to the signal path. A sampling circuit samples the DQ conductive signal path on the rising and falling edges of DQS_t/DQS_c. These samplings produce digital samples, the accuracy of which are a function of the present VrefDQ range and value. As a result of testing the accuracy of that sampling, the memory controller iteratively sets the VrefDQ range and VrefDQ value in MR6 to adjust the VrefDQ in the DDR4 SDRAM.

4.13 DQ Vref Training (cont'd)



NOTE 1 The MR command used to enter VrefDQ Calibration Mode treats MR6 A[5:0] as don't care while the next subsequent MR command sets VrefDQ values in MR6 A[5:0] .
NOTE 2 Depending on the step size of the latest programmed VREF value, Vref_time must be satisfied before disabling VrefDQ training mode.

Figure 31 — VrefDQ training mode entry and exit timing diagram

JESD79-4D, p. 60.

145. The Accused Products including DDR4 memory controllers compare the digital samples with expected values to obtain pass/fail information for each of the different values. The memory controller compares the digital samples from the DDR4 SDRAMs with the values sent to obtain an indication of whether the DDR4 SDRAM accurately sampled the DQ signals on the DQ conductive signal paths. This is done for each of the attempted VrefDQ values.

4.13.1 Example scripts for VREFDQ Calibration Mode:

When MR6 [7] = 0 then MR6 [6:0] = XXXXXXX

Entering VREFDQ Calibration if entering range 1:
- MR6 [7:6]=10 & [5:0]=XXXXXX
- All subsequent VREFDQ Calibration MR setting commands are MR6 [7:6]=10 & MR6 [5:0]=VVVVVV
  {VVVVVV are desired settings for VrefDQ}
- Issue ACT/WR/RD looking for pass/fail to determine Vcent(midpoint) as needed
- Just prior to exiting VREFDQ Calibration mode:
- Last two VREFDQ Calibration MR commands are
- MR6 [7:6]=10, MR6 [5:0]=VVVVVV' where VVVVVV' = desired value for VREFDQ
- MR6 [7]=0, MR6 [6:0]=XXXXXXX to exit VREFDQ Calibration mode

Entering VREFDQ Calibration if entering range 2:
- MR6 [7:6]=11 & [5:0]=XXXXXX
- All subsequent VREFDQ Calibration MR setting commands are MR6 [7:6]=11 & MR6 [5:0]=VVVVVV
  {VVVVVV are desired settings for VrefDQ}
- Issue ACT/WR/RD looking for pass/fail to determine Vcent(midpoint) as needed
- Just prior to exiting VREFDQ Calibration mode:
- Last two VREFDQ Calibration MR commands are
- MR6 [7:6]=11, MR6 [5:0]=VVVVVV' where VVVVVV' = desired value for VREFDQ
- MR6 [7]=0, MR6 [6:0]=XXXXXXX to exit VREFDQ Calibration mode

JESD79-4D, p. 60.

146. The Accused Products including DDR4 memory controllers based on the pass/fail information for each of the different values, select one of the values from the set for use as the parameter. Based on the pass/fail indications of the data transmission tests for the different values

of Vref DQ attempted, one value is selected for use during normal operation of the memory system after initialization and calibration is complete.

147. Additionally, the Accused Products including DDR4 memory controllers perform the aforementioned method wherein the parameter is one of a sampling phase offset, a voltage threshold offset, or an equalization setting used to produce sampled digital values from the signal. The parameter, V ref DQ is a voltage threshold offset used in sampling digital DQ values from the DQ conductive signal path.

148. Defendants have and continue to indirectly infringe one or more claims of the '511 Patent by knowingly and intentionally inducing others, including NXP customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

149. Upon information and belief, with knowledge and intent, or with willful blindness, Defendants encourage and facilitate infringement of one or more claims of the '511 Patent by others, including at least claim 1. For example, Rambus Inc. notified NXP in August 2018 that NXP was infringing the'511 Patent by making, using, selling, offering to sell, and/or importing products, including the LS1046A family, that include controllers for, DDR4 memories.

150. Defendants, with knowledge that these products, or the use thereof, infringe the '511 Patent at least as of August 2018, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the '511 Patent by providing these products to end-users for use in an infringing manner.

151. Defendants induced infringement by others, including end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability

that others, including end-users, infringe the '511 Patent, but while remaining willfully blind to the infringement.

152. Rampart has suffered damages as a result of Defendants' direct and indirect infringement of the '511 Patent in an amount to be proved at trial.

153. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendants' infringement of the '511 Patent for which there is no adequate remedy at law, unless Defendants' infringement is enjoined by this Court.

154. NXP has committed and continues to commit acts of infringement that NXP actually knew or should have known constituted an unjustifiably high risk of infringement of at least one valid and enforceable claim of the '511 Patent. NXP's direct and indirect infringement of the '511 Patent has been and continues to be willful, intentional, deliberate, and/or in conscious disregard of Rampart's rights under the patent. Rampart is entitled to an award of treble damages, reasonable attorney fees, and costs in bringing this action.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Rampart prays for relief against Defendants as follows:

a. Entry of judgment declaring that Defendants have directly and/or indirectly infringed one or more claims of each of the Patents-in-Suit;

b. An order pursuant to 35 U.S.C. § 283 permanently enjoining Defendants, their officers, agents, servants, employees, attorneys, and those persons in active concert or participation with them, from further acts of infringement of the Patents-in-Suit;

c. An order awarding damages sufficient to compensate Rampart for Defendants' infringement of the Patents-in-Suit, but in no event less than a reasonable royalty, together with interest and costs;

d. Entry of judgment declaring that this case is exceptional and awarding Rampart its costs and reasonable attorney fees under 35 U.S.C. § 285; and,

e. Such other and further relief as the Court deems just and proper.

Dated: December 13, 2021

Respectfully submitted,

/s/ Raymond W. Mort, III

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